ABSTRACT OF THE DISCLOSURE

A method and circuit for refreshing dynamic memory cells arranged along word lines and bit lines are provided, the memory cells being refreshed in a manner dependent on a refresh signal with a refresh frequency by the activation of the word line in order to write the information back to the memory cells arranged on the relevant word line, in which case the refresh frequency is set in a manner dependent on the charge loss of first dummy memory cells during a refresh period of the refresh signal on a first dummy word line and/or in a manner dependent on the charge loss of second dummy memory cells during the refresh period of the refresh signal on a second dummy word line.